METHOD AND APPARATUS FOR INTERFACING A PROCESSOR TO A COPROCESSOR

Abstract

The present invention relates generally to interfacing a processor with at least one coprocessor. One embodiment relates to a processor having a set of broadcast specifiers which it uses to selectively broadcast an operand that is being written to a register within the processor to a coprocessor communication bus. Each broadcast specifier may therefore include a broadcast indicator corresponding to each general purpose register of the processor. An alternate embodiment may also use the concept of broadcast regions where each broadcast region may have a corresponding broadcast specifier where one broadcast specifier may correspond to multiple broadcast regions. Alternatively, in one embodiment, the processor may use broadcast regions independent of the broadcast specifiers where the coprocessor is able to alter its functionality in response to the current broadcast region. In one embodiment, the processor may provide a region specifier via the coprocessor communication bus to indicate the current broadcast region.